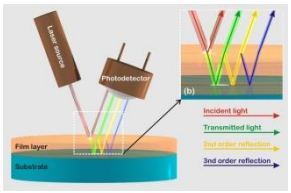
ThetaMetrisis APPLICATION NOTE #038

Fast & Accurate mapping of layers thicknesses of SOI wafers



Introduction:

Silicon On Insulator (SOI) wafers are widely used for MEMS (MicroElectronic-Mechanical-Systems), and CMOS integrated circuit fabrication purposes. The use of an insulating layer between the silicon substrate and the supper layer of silicon, improves the performance of the devices over ones on conventional silicon substrates by reducing electrical losses. SOI wafers have greater resistance to radiation, making them less prone to soft errors. The higher density also increases the yield, thus improving wafer utilization. Additional advantages of SOI wafers include a reduced dependency on temperature and fewer antenna issues. In the case of MEMS, the buried oxide allows for the realization of suspended membranes with unique characteristics. In this application note, a **ThetaMetrisis FR-Scanner** is employed for thickness mapping of the three layers of an SOI wafer.

Means & Methods:

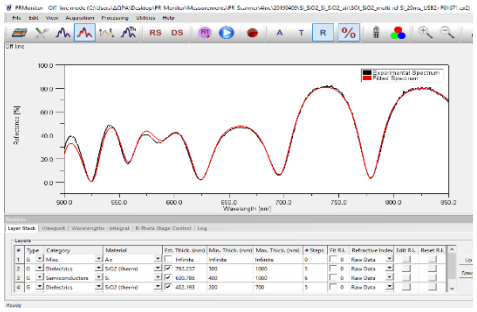
Samples under investigation was a 4inch SOI wafer with a thermal SiO_2 layer on top: ***SiO_2/Si/SiO_2/Si***. All measurements were performed by a **FR-Scanner** tool operating at the spectral range of **370-1020nm**, able to measure thickness of coatings from **12nm up to 90um**. The tool scans the samples under test in very high speed by rotating the stage and by moving linearly the optical head on top (polar scanning) and without bending of the reflection probe. The pattern generated through **FR-Monitor** includes (in case of 4inch wafer) 169 points in (R, theta) positions, and the scan lasted **less than 30sec**.

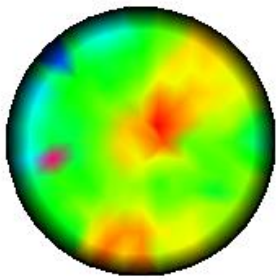
Results:

In the images below, typical recorded reflectance spectra (black line) and fitted reflectance spectra (red line), as seen on the FR-Monitor software, of all layers on random points, are illustrated along with the mapping profiles of each layer. The thickness of all three layers was measured simultaneously. The color code guides the eye on the thickness uniformity of each layer and numerous statistical data are provided such as: standard deviation, mean thickness value, qualified points against a criterion set by the user etc.

Layer 1

*Dielectric top Layer (**SiO_2 Layer**)*





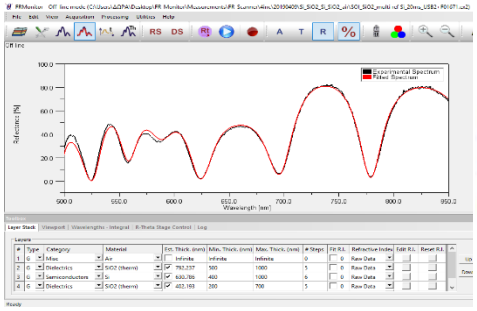
Average Thickness =
794.10 nm

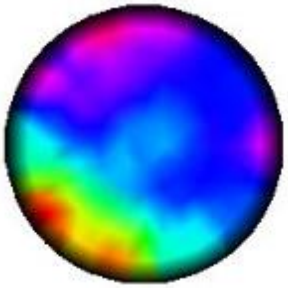
Standard Deviation =
1.370

Qualified Samples =
120/168 (71.4%)

Layer 2

*Device Layer (**Si Layer**)*





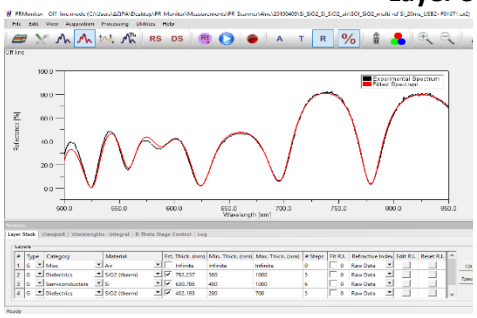
Average Thickness =
630.56 nm

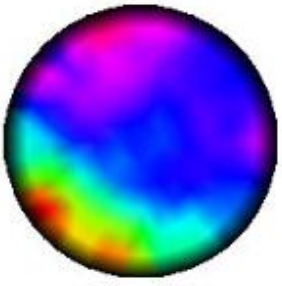
Standard Deviation =
1.774

Qualified Samples =
120/168 (71.4%)

Layer 3

BOX
*(**SiO_2 Layer**)*





Average Thickness =
400.82 nm

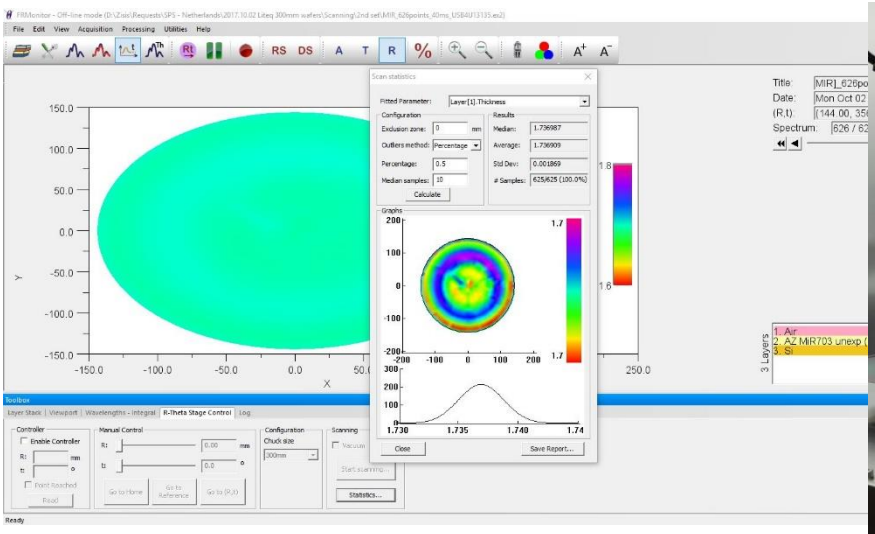
Standard Deviation =
3.839

Qualified Samples =
120/168 (71.4%)

For the calculation of the statistical parameters and the representation of the point distribution, some points can be excluded, according the statistics calculation parameters. These excluded points are considered as “extreme” points, which can alter the statistics in the unwanted way, so the user can exclude them. For example, in the mapping profile of ***Device Layer (Si layer)*** presented above, 120 of 168 points are included in that range, so the qualified region of the wafer represents the 71.4% of its total area, indicated with color in the 2D graphs.

Conclusions:

Thickness mapping of all layers simultaneously (SiO_2 and Si ones) of an SOI wafer was evaluated by using a FR-Scanner. FR-Scanner is the fast and accurate solution for characterization of single films or stack of films over large areas or preselected positions through scanning.



Screenshot of the FR-Monitor software

Image of FR-Scanner